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Fully Transparent Thin-Film Transistor Devices Based on SnO_2 Nanowires

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ABSTRACT

We report on studies of field-effect transistor (FET) and transparent thin-film transistor (TFT) devices based on lightly Ta-doped SnO_2 nanowires. The nanowire-based devices exhibit uniform characteristics with average field-effect mobilities exceeding 100 $cm^2/V \cdot s$. Prototype nanowire-based TFT (NW–TFT) devices on glass substrates showed excellent optical transparency and transistor performance in terms of transconductance, bias voltage range, and on/off ratio. High on-currents and field-effect mobilities were obtained from the NW–TFT devices even at low nanowire coverage. The SnO_2 nanowire-based TFT approach offers a number of desirable properties such as low growth cost, high electron mobility, and optical transparency and low operation voltage, and may lead to large-scale applications of transparent electronics on diverse substrates.

Semiconductor nanowires (NWs) have attracted increasing interest in the last a few years and are expected to lead to novel device applications.[1−3] In particular, it has been shown recently that high-performance nanowire-based thin-film transistor (TFT) devices can be fabricated on a variety of substrates including glass and plastics.[4−7] The key advantage of the NW−TFT approach compared to conventional TFT techniques is the clear separation of the device fabrication stage from the material growth stage, such that there is no longer need to be concerned with compatibility with the *device* substrate during growth, and high growth temperature can be used to obtain crystalline materials. Specifically, the synthesis of NW building blocks is first carried out under conditions optimized to yield high-quality single-crystal materials, where the desired electronic and/or optoelectronic properties are defined by material composition, structure, and size. The NWs are then transferred from the growth substrate onto the desired device substrate and configured into a thin-film form, followed by conventional fabrication processes to produce TFT devices.[4,5]

In previous studies on NW−TFT devices, the channel was typically formed by opaque semiconductor nanowires, such as silicon, and the source, drain, and gate electrodes were made of normal metals such as Au or Ni.[4−6] On the other hand, high-performance optically transparent TFTs will lead to new frontiers such as "invisible electronics" and are of great current interest. Here we report fully transparent TFT devices based on SnO_2 nanowire films and indium tin oxide (ITO) electrodes. Key performance metrics including mobility, on/off ratio, and operating voltages of the SnO_2 NW−TFT devices fabricated on glass substrates are similar to those of individual nanowires and are better than those of conventional metal oxide TFTs fabricated near room temperature.[8,9] The performance metrics are also comparable with or better than conventional transparent TFTs using single-crystalline channel materials, which typically require high-temperature growth/annealing and expensive single-crystalline substrates.[10−14]

SnO_2 nanowires were chosen in our studies due to the low growth cost, high optical transmittance, and the ease of obtaining Ohmic contacts with conventional transparent conducting oxide films. Particularly, single-crystalline SnO_2 nanowires may be grown using a simple vapor transport synthesis method that allows for the growth of large quantities of nanowires at a cost lower than that of indium-based metal oxide materials[15] or silicon nanowires and carbon nanotubes.[16] Previous studies on SnO_2 nanowire or nanobelt structures, however, have focused on undoped materials in which the carriers (electrons) were provided by deviation from stoichiometry (in the form of oxygen vacancies) or unintentional doping by (uncontrolled) impurities in the growth facility.[17−19] The undoped nanowire samples typically

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exhibit low carrier concentrations and are very sensitive to changes in ambient conditions. These properties, desirable for environmental sensors,[19] are nonetheless detrimental for high-performance transistor device applications. To address this problem, we have recently developed a reliable in situ doping process that has been shown to dramatically affect the nanowires' electrical properties in a controlled fashion.[16,20] For instance, degenerately Sb-doped SnO_2 nanowires have been demonstrated to exhibit resisitivites as low as the best thin-film samples and show metal-like behavior.[16] In this work, we focus on lightly Ta-doped SnO_2 nanowires that serve as the channel material in nanowire FET and TFT devices. The Ta-doped SnO_2 nanowires were synthesized on (100) Si substrates by a catalyst-mediated vapor−liquid−solid (VLS) process[16,20,21] in which the Ta and Sn source materials were provided by a vapor transport method.[16,20] Briefly, high-purity (99.99%) powders containing the source materials (Sn:Ta = 95:5 in weight ratio) were first mixed thoroughly and loaded in an alumina boat. The (100) Si growth substrates were sputter-deposited with 5 nm of Au film, serving as the catalysts in the VLS process, and were placed on top of the boat. The alumina boat was then loaded into an alumina reactor tube positioned inside a horizontal tube furnace. During growth, the furnace was heated from room temperature to 900 °C at a rate of 20 °C/min under Ar flow (500 sccm) with a trace amount of oxygen. The growth time was 1 h at 900 °C, followed by cool down to room temperature at a rate of 5 °C/min.

Figure 1a shows a low-magnification scanning electron microscopy (SEM) image of the as-synthesized sample. Large quantities of nanowires were observed only in the areas covered with Au catalysts. The nanowires have a mean lateral size of 55 nm and are typically tens of micrometers long. Structural properties of the nanowires were further investigated with transmission electron microscopy (TEM) studies. Figure 1b shows a low-magnification TEM image of a single Ta-doped SnO_2 nanowire with lateral size of ca. 60 nm, illustrating the uniform lateral size and lack of tapering along the growth direction. The crystallography of the nanowires was studied by select area electron diffraction (SAED) (upper inset, Figure 1b) and HRTEM imaging (lower inset, Figure 1b). These results show that the Ta-doped SnO_2 nanowires have a tetragonal rutile crystal structure ($a = 0.474$ nm, and $c = 0.318$ nm). HRTEM studies also verify that each Ta-doped SnO_2 nanowire is a perfect single crystal with no visible dislocations and amorphous surface overcoating. The growth direction of the Ta-doped SnO_2 nanowire shown in Figure 1b was determined to be [101] based on the analysis of the diffraction pattern.

After growth, the nanowires were transferred to the corresponding device substrates and a number of device structures were fabricated and tested. Unless noted otherwise, all electrical measurements were carried out in air at room temperature. Single-nanowire-based FETs with a standard back-gated structure were studied first to investigate the intrinsic electrical properties of the Ta-doped SnO_2 nanowires. The device fabrication involves removing the nanowires from the Si growth substrate by sonication in isopropyl

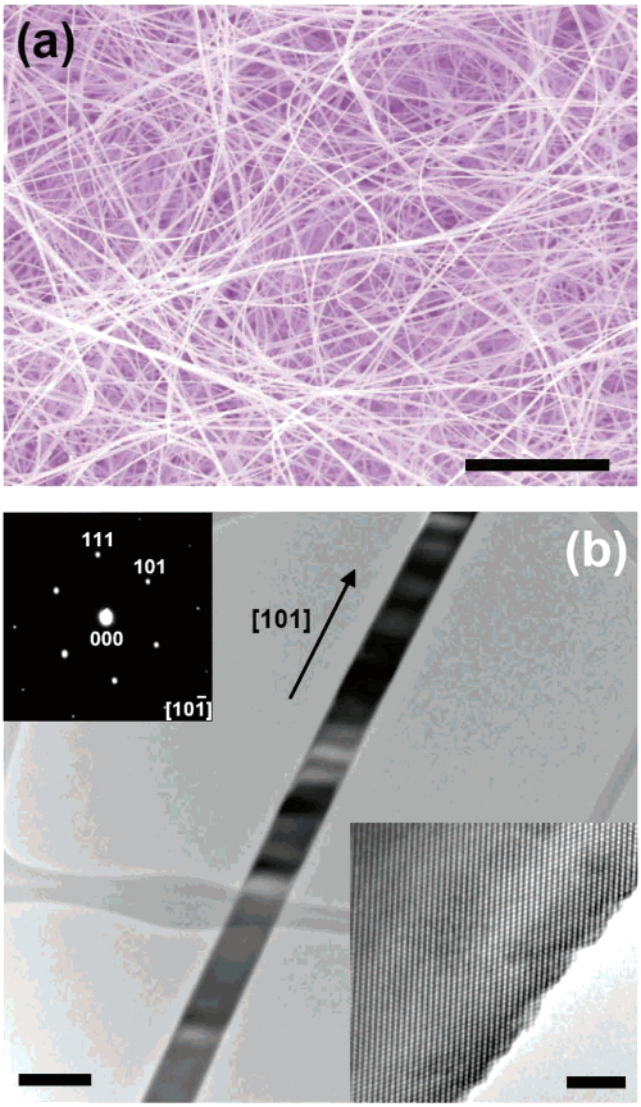

Figure 1. Structural characterization of the Ta-doped SnO_2 nanowires. (a) SEM image of the as-grown nanowires displaying the high-growth density. Scale bar: 2 μm. (b) Low-magnification TEM image of a single Ta-doped SnO_2 nanowire with lateral size of ca. 60 nm. Scale bar: 100 nm. Top inset: select area electron diffraction (SAED) pattern of the SnO_2 nanowire. Bottom inset: HRTEM image of the same SnO_2 nanowire. Scale bar: 5 nm.

alcohol and nanowire deposition onto a degenerately doped n^+ silicon substrate capped with a 50 nm silicon dioxide (SiO_2) layer by drop drying. Photolithography was then used to define pairs of source/drain electrodes to contact each nanowire, followed by the metal deposition of Ti/Au (10/100 nm) by electron beam evaporation to complete the device structure, with the n^+ Si substrate serving as the back gate (Figure 2a, inset).

The Ta-doped SnO_2 nanowire FETs were found to exhibit standard n-type transistor behavior. Doping of the SnO_2 nanowires also helps to reduce contact resistance in the FET devices, as evidenced by the apparent absence of Schottky behavior in the current−voltage ($I_{ds}-V_{ds}$) characteristics (Figure 2b). In contrast, our control experiments on undoped SnO_2 nanowires showed pronounced Schottky barrier behavior (Figure S1, Supporting Information), consistent with

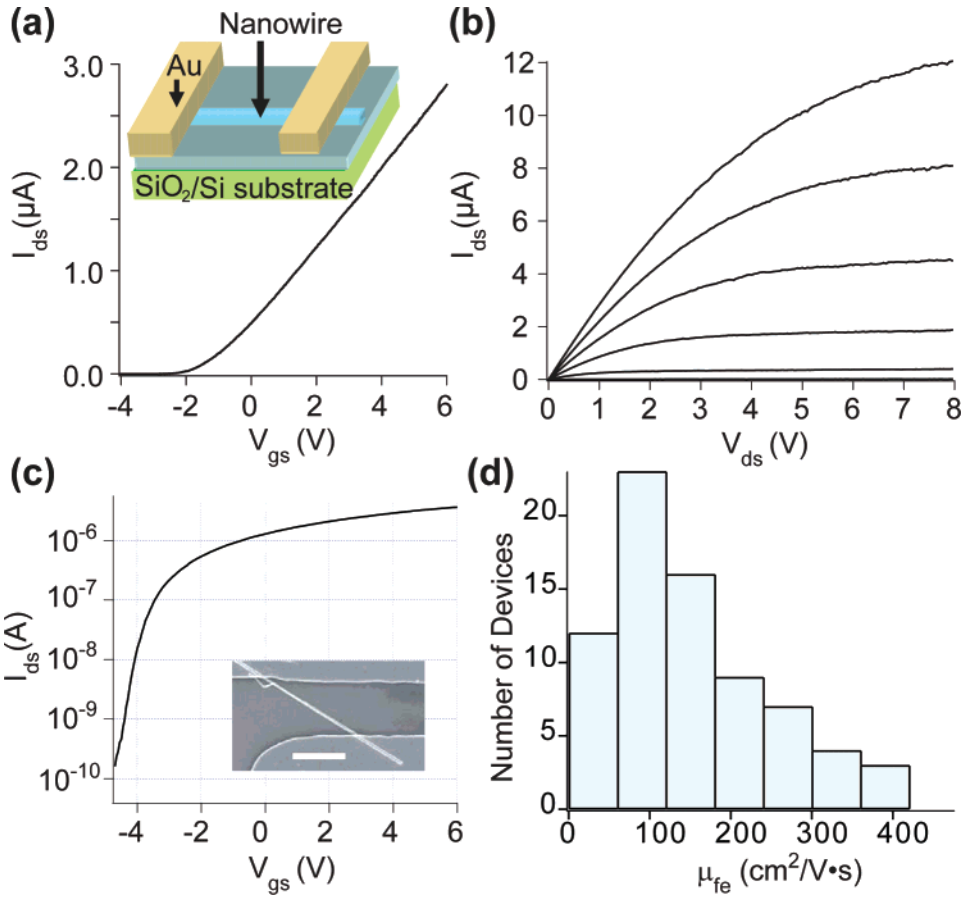

Figure 2. Transistor characteristics of back-gated Ta-doped SnO_2 nanowire FET devices on silicon substrates. (a) Current (I_{ds}) vs gate voltage (V_{gs}) curve at linear region ($V_{ds} = 1$V) for a back-gated NW−FET. Inset: schematic of the device. (b) Family of $I_{ds}-V_{ds}$ curves for the same device with $V_{gs} = 6$ to -4 V in -2 V steps from top to bottom. (c) $I_{ds}-V_{gs}$ curve in log scale at $V_{ds} = 1$V. The subthreshold slope S was estimated to be 270 mV/decade. Inset, SEM image of the device. Scale bar: 2 μm. (d) Histogram of the extracted field-effect mobilities (μ_{fe}) for 75 devices.

earlier studies.[18,19] The field-effect mobility μ_{fe} of the device in Figure 2 was estimated using the equation

$$g_m = \frac{\mu_{fe} C_g}{L^2} V_{ds} \quad (1)$$

in the linear operation regime. Here $g_m = dI_{ds}/dV_{ds}$ is the linear-region transconductance, and $L = 4.95$ μm is the nanowire device channel length. C_g is the capacitance of the back gate and can be estimated by utilizing the cylinder-on-plane model:

$$C_g = \frac{2\pi\epsilon_r\epsilon_0}{\cosh^{-1}\left(\frac{2h+d}{d}\right)} L \quad (2)$$

where ϵ_0 is the vacuum dielectric constant, $h = 50$ nm is the thickness of the SiO_2 layer, and $d = 87$ nm is the lateral size of the nanowire. ϵ_r is the relative dielectric constant and was chosen to be 2.5, which is the average of air (1) and SiO_2 (3.9). We note eq 2 evolves into the commonly used capacitance model[22] $C_g = 2\pi\epsilon_r\epsilon_0/\ln(4h/d)$ when $h \gg d$, and the estimated capacitance value of 100 aF/μm using eq 2 also agrees well with results obtained from finite element simulations. Using the estimated capacitance value and measured device parameters, μ_{fe} of the device in Figure 2 was estimated to be 120 cm^2/(V•s) in the linear bias region. Other device parameters were also obtained in transport studies. The subthreshold slope S was estimated to be 270 mV/decade and independent of the bias voltage. An on/off ratio of $>10^5$ was achieved within the 10 V bias range. Finally, the maximum transconductance was obtained in saturation and was found to be 2.94 μS at $V_{ds} = 10$ V. The histogram of the extracted μ_{fe} for 75 devices was plotted in Figure 2d with an average μ_{fe} value of 156 cm^2/V•s. We note this value is consistent with those obtained in planar single-crystalline SnO_2 samples[23] and other metal oxide nanowires.[24]

To demonstrate the potential of Ta-doped SnO_2 nanowires as transparent devices, we further fabricated nanowire transistors on glass substrates in which the back-gate, source, and drain electrodes were replaced with transparent conducting Sn-doped In_2O_3 (ITO) films (Figure 3a, inset). Briefly, an ITO film with thickness of ca. 250 nm was first deposited on a glass substrate (Fisherbrand, 2.5 cm × 2.5 cm, 250 μm thick) by pulsed laser deposition (PLD) at 400 °C, followed by the SiO_2 gate dielectric layer (75 nm thick) deposition

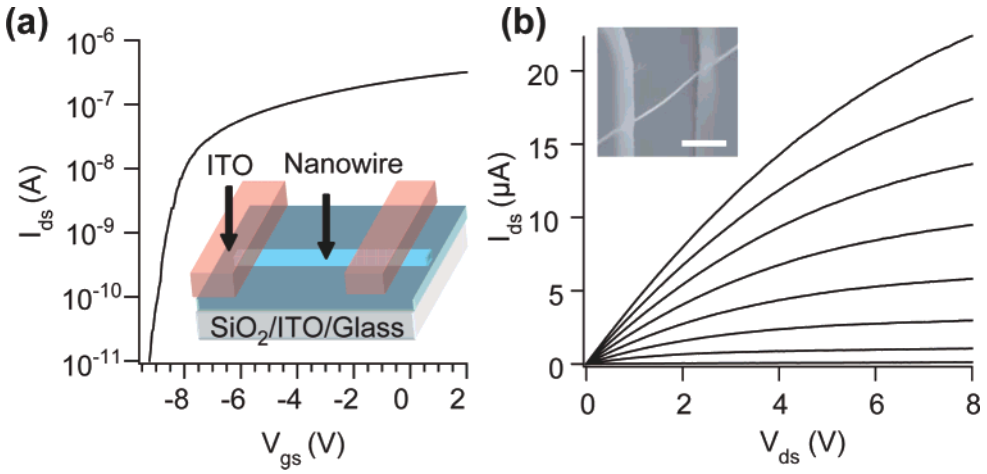

Figure 3. Transistor characteristics of a back-gated transparent Ta-doped SnO_2 nanowire FET on glass with ITO contacts. (a) $I_{ds}-V_{gs}$ curve in the linear region ($V_{ds} = 0.1$ V). The subthreshold slope S was estimated to be 312 mV/decade, and μ_{fe} was estimated to be 178 $cm^2/V\cdot s$. Inset, schematic of the device. (b) Family of $I_{ds}-V_{ds}$ curves for the same device with $V_{gs} = 6$ to -8 V in -2 V steps from top to bottom. Inset: SEM image of the device. Scale bar: 2 μm.

via plasma-enhanced chemical vapor deposition (PECVD). The bottom ITO layer and SiO_2 layer serve as the back-gate and dielectric, respectively. Single-nanowire transistor devices were then fabricated on the SiO_2/ITO/glass substrate in the same fashion as the back-gated device in Figure 2, except that the source/drain electrodes were replaced by 200 nm thick PLD deposited ITO films.

The devices on glass substrates show transmittances of ~80% in the visible light range of 380−800 nm (Figure S2, Supporting Information). Significantly, no performance degradation was observed on devices fabricated on glass substrates with ITO electrodes. As seen in Figure 3b, linear $I_{ds}-V_{ds}$ behavior was still observed at small bias, indicating Ohmic contacts with ITO source/drain electrodes. At high bias, "hard saturation" was once again observed for the transparent FET, with a saturation transconductance $g_m = 2.27$ μS measured at $V_{ds} = 10$ V. The on/off ratio and subthreshold slope S were inferred from Figure 3a to be 10^5 and 312 mV/decade, respectively. The field-effect mobility μ_{fe} was estimated to be 179 $cm^2/V\cdot s$ in the linear region. These values are consistent with those obtained on devices fabricated on silicon substrates with Ti/Au S/D electrodes (e.g., the device in Figure 2) and clearly demonstrate the potential of SnO_2 nanowires in fully transparent electronics applications.

Following studies on single-nanowire devices, fully transparent thin-film transistors were fabricated on glass substrates using arrays of parallel Ta-doped SnO_2 nanowires as the transistor channel with a staggered top-gated TFT design (Figure 4b). Aligned Ta-doped SnO_2 nanowires were transferred onto a Pyrex glass substrate (500 μm thick) with surface coverage of at least 25% (Figure 4a) using a physical transfer method.[5] Conventional sputter, photolithography, and liftoff processes were used to pattern the device structure. Several improvements were made compared to the back-gated devices to improve the device performance and to facilitate large-scale applications. First, we note that PLD likely will not be a scalable technique to fabricate the ITO electrodes for large scale TFT devices. Second, the deposition temperatures of the ITO films and the SiO_2 dielectric (both at 400 °C) are too high for device applications on plastic substrates. To address these issues, sputter-deposited ITO films and SiO_2 dielectric were used. The ITO films were deposited by RF sputtering using an In_2O_3/SnO_2 target (90/10 by wt) at 400 W without substrate heating. Afterward the ITO films were annealed at 250 °C inside a furnace to improve the conductivity and transparency. The SiO_2 dielectric was deposited by RF sputtering using a SiO_2 target at 700 W without substrate heating or annealing. The TFT devices fabricated using this approach are still highly transparent in the visible range, as shown in Figure 4c,d, with a transmittance of ~70%, including the pyrex glass substrate. Significantly, the highest temperature in the TFT fabrication process was limited to 250 °C in our approach, making this approach compatible with certain plastic substrates for applications of transparent, flexible electronics.

The single-crystalline channel of the nanowire-based TFT devices affords excellent performance metrics. Electrical characterizations obtained on a top-gated NW−TFT device with a W/L ratio of 12.6 ($W = 48$ μm, $L = 3.8$ μm) are shown in Figure 5. The device displays enhancement-mode n-type transistor behavior, with clear linear and saturation regions observed in the $I_{ds}-V_{ds}$ output curves (Figure 5b). Significantly, a large on current $I_{on} = 71$ μA, transconductance of 49 μS, and on/off ratio ~10^3 can be obtained within a small V_{dd} bias window of 2.5 V (with V_{gs} from 3.5 to 6 V and $V_{ds} = 2.5$ V). Compared with amorphous or polycrystalline transparent TFT devices fabricated near room temperature, the NW−TFT device shows better performance within a smaller V_{dd} bias window.[8,9] The subthreshold slope S was measured to be 538 mV/decade from Figure 5c. This value is comparable with that obtained in silicon nanowire TFTs[4] and may be further improved by improving the nanowire/dielectric interface or using high-k dielectrics.[15,25,26] Figure 5c also shows that the device exhibits a small gate leakage of less than 10 nA within the bias window, and negligible drain-induced barrier-lowering (DIBL) effects.

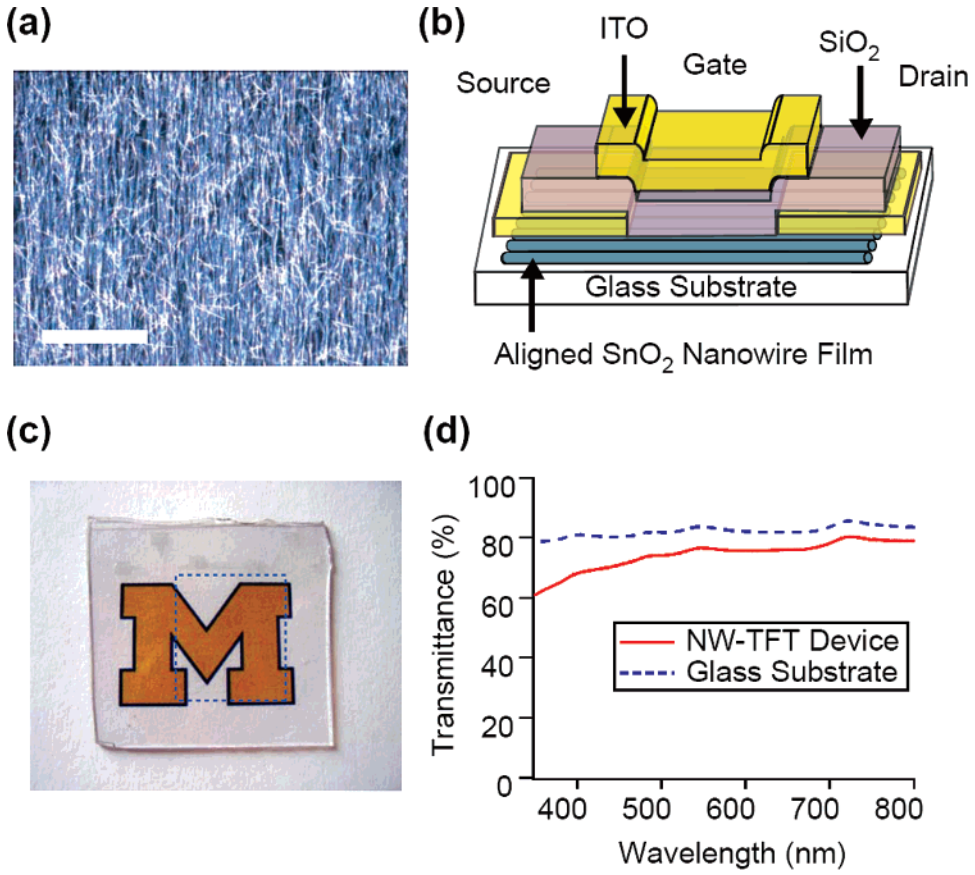

Figure 4. Structure of the NW−TFT devices. (a) Dark-field optical microscope image of a SnO_2 nanowire film obtained through the physical transfer method. Scale bar: 20 μm. (b) Schematic of the transparent SnO_2 nanowire-based TFT device, showing the ITO source/drain and gate electrodes, and the staggered transistor structure. (c) Digital photograph of a 200-device array of NW−TFTs fabricated on 500 μm thick Pyrex glass. The logo of University of Michigan can be clearly seen through the NW−TFT array. The dashed region illustrates the device array area. (d) Optical transmittance spectrum of the NW−TFT device array on glass substrate (solid line) and the glass substrate alone (dashed line).

The field-effect mobility (μ_{fe}) of this TFT device can be estimated using eq 1 by noting that C_g is now the total gate capacitance of the TFT device. A conservative estimate of $C_g = C_0 \times (W \times L)$ was used in our estimate, corresponding to the ideal case of full nanowire coverage. Here C_0 is the capacitance per unit area using a parallel plate model $C_0 = \epsilon_r\epsilon_0/d = 265.5\text{aF}/\mu\text{m}^2$, and $W = 48$ μm, $L = 3.8$ μm are the *physical* device width and length, respectively. With the estimated C_g values and measured device parameters, μ_{fe} was estimated to be 145 $\text{cm}^2/\text{V}\cdot\text{s}$ in the linear region and 112 $\text{cm}^2/\text{V}\cdot\text{s}$ in the saturation region.

The mobility values estimated using the conservative parallel-plate model are in fact very close to the average mobility value obtained on individual NW devices. This result was unexpected at first sight considering the capacitance obtained from the parallel-plate model assuming 100% nanowire coverage may overestimate the actual gate capacitance due to the ~25% nanowire coverage observed for the device in Figure 5. Here the term nanowire coverage denotes the ratio of the area covered by the transferred nanowires to that of the physical channel area ($W \times L$). To address this apparent discrepancy, we performed electrostatic simulations (Figure 5d) using measured parameters of the fabricated NW−TFT device structure (130 nm thick SiO_2 gate dielectric was used for the device in Figure 5). Our study verified that the estimated C_g value using the parallel plate model is in fact within 89% of the more exact C_g value obtained from electrostatic simulations when the nanowire coverage exceeds 25%. This observation can be attributed to the fact that, above a certain threshold, the nanowire array can effectively screen the field lines from the gate just as in the continuous film case (Figure 5d).[27] Because the TFT drain current (I_{ds}) and transconductance (g_m) are directly related to C_g, one can conclude that increasing the nanowire coverage above 25% in the present device structure will have little effect on the TFT performance. Looking at this problem from a different angle, the measured transconductance g_m (therefore μ_{fe}) for a NW−TFT composed of N parallel NWs can be rewritten as the sum of the transconductance from N individual NW devices:

$$g_m = N\frac{\mu_{fe}C_w}{L^2}V_{ds} \tag{3}$$

assuming the nanowires are identical. Here C_w corresponds to the effective gate capacitance for a single-nanowire (cf. eq 1). The unexpected device performance can be explained by noticing the fact that the effective gate capacitance per wire C_w decreases with nanowire coverage. Qualitatively, in the extreme case when only one wire forms the channel,

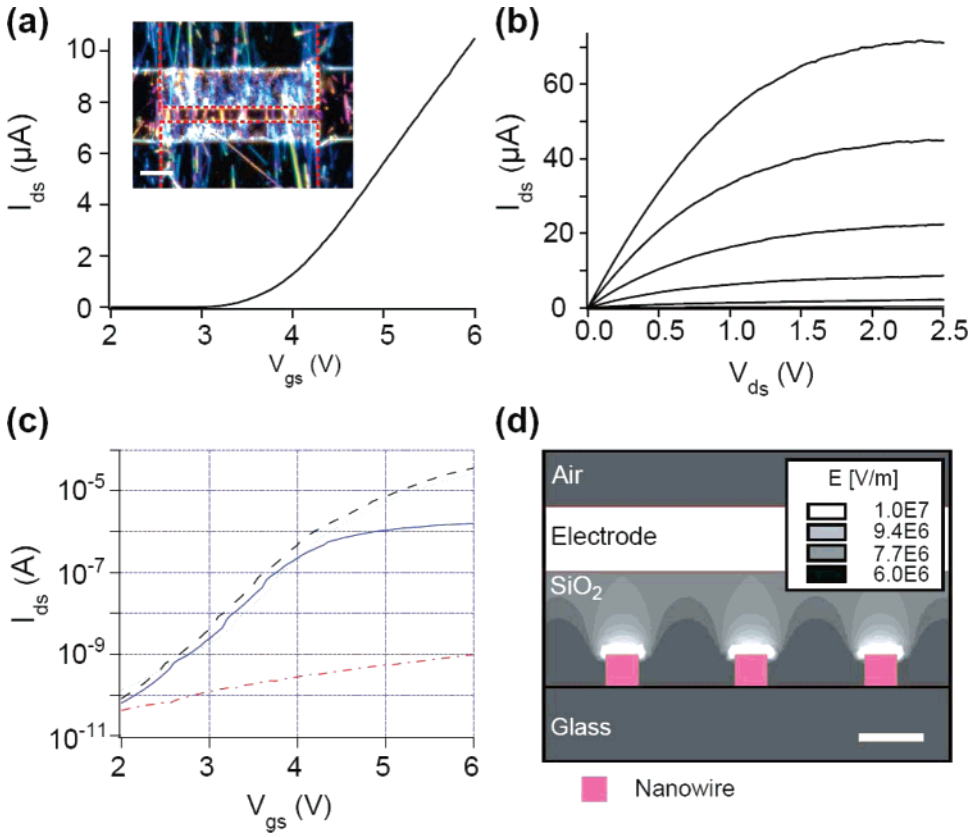

Figure 5. Electrical characterization of a transparent NW−TFT device on glass. (a) $I_{ds}-V_{gs}$ curve at $V_{ds} = 0.1$V. μ_{fe} was estimated to be 145 $cm^2/V\cdot s$. Inset, optical dark-field microscope image of the device. The dashed lines highlight the source and drain electrodes. Scale bar: 10 μm. (b) Family of $I_{ds}-V_{ds}$ curves for the same device with $V_{gs} = 6$ to 3.5 V in −0.5 V steps. (c) I_{ds} vs V_{gs} curve in log scale for $V_{ds} = 0.1$ V (blue solid line) and 3 V (black dashed line). The gate leakage current I_{gs} at $V_{ds} = 1$ V was also plotted (red dash−dotted line). The subthreshold slope S was estimated to be 538 mV/decade. (d) Distribution of the electrical fields in the cross-section of a NW−TFT with 25% nanowire coverage obtained through electrostatic simulation (Maxwell Ansoft 2D, version 11) at $V_{gs} = 1$ V.

field lines from the NW extends over the whole gate area and C_w is determined by eq 2 from the cylinder-on-plane model. In other words, the effective capacitor area A is much larger than the size of the nanowire itself. As N and the nanowire coverage increases, the field lines from each nanowire are confined to smaller areas (e.g., Figure 5d). As a result, the effective capacitor area A for each nanowire decreases, resulting in smaller C_w. Above a certain nanowire coverage, the effects of increasing N and decreasing C_w almost completely cancel each other, and the performance metrics of the NW−TFT device will no longer improve with increased nanowire coverage.

This observation has important consequences in nanowire-based electronics, as it shows that nanowire arrays produced using less-than-optimal assembly techniques with relatively low coverage can still act effectively as thin-film devices. Figure 6 shows the calculated gate capacitance C_g as a function of the nanowire coverage at different oxide thickness conditions. For relatively thick gate dielectric thicknesses (blue squares) that can be readily produced with inexpensive, scalable techniques such as sputtering, a nanowire film with low surface coverage will behave similarly to a continuous planar single-crystalline thin-film of the same material and thickness. To take advantage of higher coverage (denser) nanowires as the TFT channel, thinner gate dielectrics or high-k materials will have to be used so that the gate is more effectively coupled to the nanowire array (red circles, Figure 6).

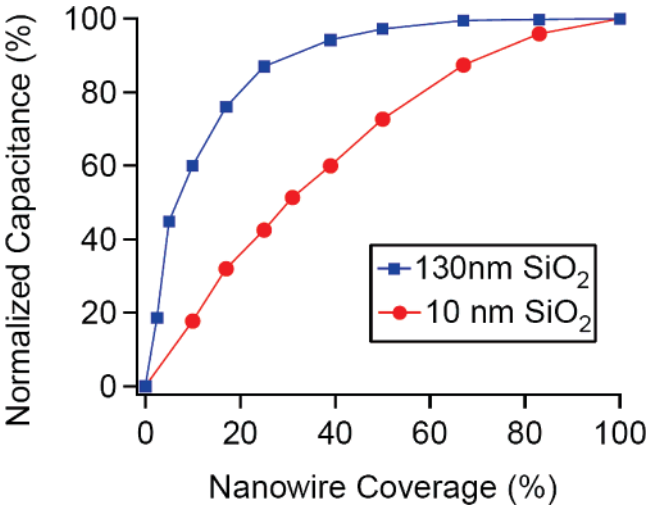

Figure 6. Gate capacitance of the NW−TFT as a function of the nanowire coverage in the channel region at different dielectric thicknesses. The gate capacitance is normalized to the maximum value when the nanowire coverage is 100%.

In conclusion, single-crystalline Ta-doped SnO_2 nanowires were obtained using a simple low-cost growth method.

Electrical characterizations on single-nanowire devices show that the nanowires can serve as channel materials in transparent transistor devices with field-effect mobilities over 100 $cm^2/V \cdot s$. Transparent NW−TFT devices were produced near room temperature and were found to exhibit similar high-mobility values even at low nanowire coverage. This study may lead to large-scale applications of high-performance transparent nanowire-based thin-film devices on diverse substrates such as flexible electronics on plastics.

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Supporting Information Available: $I_{ds}-V_{ds}$ curve of undoped SnO_2 devices, optical transmittance spectrum of an array of bottom-gated single-nanowire transistor device on glass, and optical micrograph of array of the top-gated NW−TFT structure. This material is available free of charge via the Internet at http://pubs.acs.org.

References

(1) Lieber, C. M. *MRS Bull.* **2003**, *28*, 486.
(2) Thelander, C.; Agarwal, P.; Brongersma, S.; Eymery, J.; Feiner, L. F.; Forchel, A.; Scheffler, M.; Riess, W.; Ohlsson, B. J.; Gosele, U.; Samuelson, L. *Mater. Today* **2006**, *9*, 28.
(3) Wang, Z. L. *Mater. Today* **2004**, *7*, 26.
(4) Duan, X. F.; Niu, C. M.; Sahi, V.; Chen, J.; Parce, J. W.; Empedocles, S.; Goldman, J. L. *Nature* **2003**, *425*, 274.
(5) Javey, A.; Nam, S.-W.; Friedman, R. S.; Yan, H.; Lieber, C. M. *Nano Lett.* **2007**, *7*, 773.
(6) McAlpine, M. C.; Friedman, R. S.; Jin, S.; Lin, K.-h.; Wang, W. U.; Lieber, C. M. *Nano Lett.* **2003**, *3*, 1531.
(7) Tao, A.; Kim, F.; Hess, C.; Goldberger, J.; He, R.; Sun, Y.; Xia, Y.; Yang, P. *Nano Lett.* **2003**, *3*, 1229.
(8) Nomura, K.; Ohta, H.; Takagi, A.; Kamiya, T.; Hirano, M.; Hosono, H. *Nature* **2004**, *432*, 488.
(9) Fortunato, E. M. C.; Barquinha, P. M. C.; Pimentel, A. C. M. B. G.; Gonçlves, A. M. F.; Marques, A. J. S.; Pereira, L. M. N.; Martins, R. F. P. *Adv. Mater.* **2005**, *17*, 590.
(10) Dehuff, N. L.; Kettenring, E. S.; Hong, D.; Chiang, H. Q.; Wager, J. F.; Hoffman, R. L.; Park, C.-H.; Keszler, D. A. *J. Appl. Phys.* **2005**, *97*, 064505.
(11) Chiang, H. Q.; Wager, J. F.; Hoffman, R. L.; Jeong, J.; Keszler, D. A. *Appl. Phys. Lett.* **2005**, *86*, 013503.
(12) Presley, R. E.; Munsee, C. L.; Park, C.-H.; Hong, D.; Wager, J. F.; Keszler, D. A. *J. Phys. D* **2004**, *37*, 2810.
(13) Hoffman, R. L.; Norris, B. J.; Wager, J. F. *Appl. Phys. Lett.* **2003**, *82*, 733.
(14) Nomura, K.; Ohta, H.; Ueda, K.; Kamiya, T.; Hirano, M.; Hosono, H. *Science* **2003**, *300*, 1269.
(15) Wang, L.; Yoon, M.-H.; Lu, G.; Yang, Y.; Facchetti, A.; Marks, T. J. *Nat. Mater.* **2006**, *5*, 893.
(16) Wan, Q.; Dattoli, E. N.; Lu, W. *Appl. Phys. Lett.* **2007**, *90*, 222107.
(17) Liu, Z.; Zhang, D.; Han, S.; Li, C.; Tang, T.; Jin, W.; Liu, X.; Lei, B.; Zhou, C. *Adv. Mater.* **2003**, *15*, 1754.
(18) Hernandez-Ramirez, F.; Tarancon, A.; Casals, O.; Rodriguez, J.; Romano-Rodriguez, A.; Morante, J. R.; Barth, S.; Mathur, S.; Choi, T. Y.; Poulikakos, D.; Callegari, V.; Nellen, P. M. *Nanotechnology* **2006**, *17*, 5577.
(19) Arnold, M. S.; Avouris, P.; Pan, Z. W.; Wang, Z. L. *J. Phys. Chem. B* **2003**, *107*, 659.
(20) Wan, Q.; Dattoli, E. N.; Fung, W. Y.; Guo, W.; Chen, Y.; Pan, X.; Lu, W. *Nano Lett.* **2006**, *6*, 2909.
(21) Lu, J. G.; Chang, P. C.; Fan, Z. Y. *Mater. Sci. Eng. R* **2006**, *52*, 49.
(22) Cui, Y. Y.; Duan, X.; Hu, J.; Lieber, C. M. *J. Phys. Chem. B* **2000**, *104*, 5213.
(23) Gordon, R. G. *MRS Bull.* **2000**, *25*, 52.
(24) Li, C.; Zhang, D. H.; Han, S.; Liu, X. L.; Tang, T.; Zhou, C. W. *Adv. Mater.* **2003**, *15*, 143.
(25) Klauk, H.; Zschieschang, U.; Pflaum, J.; Halik, M. *Nature* **2007**, *445*, 745.
(26) Xiang, J.; Lu, W.; Hu, Y.; Wu, Y.; Yan, H.; Lieber, C. M. *Nature* **2006**, *441*, 489.
(27) We note that after we finished drafting the manuscript and performed all the experimental and analytical work, an independent study was published discussing similar effects on arrays of aligned carbon nanotubes (Kang, S. J.; Kocabas, C.; Ozel, T.; Shim, M.; Pimparkar, N.; Alam, M. A.; Rotkin, S. V.; Rogers, J. A. *Nat. Nanotechnol.* **2007**, *2*, 230).

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